Things to do in Lab 5.

1. Schematic of **1-bit full adder** using logic gates. **Test bench** using Verilog to test your circuit.
2. Create a symbol for 1-bit adder ( Tools->Symbol Wizard, then select your design). Use the 1-bit full adder block to create the **4-bit ripple carry full adder** in schematics.
3. Use the 1-bit full adder symbol and create **4-bit carry-look-ahead adder** in schematics.  Note that, unlike ripple carry adder where you connect the carry\_out of the previous block to carry\_in of the next, you will be using the input bits to directly generate the carry\_in for all the blocks (see manual for the logic equations). The carry\_outs of the blocks will be unconnected except the leftmost block which now becomes the carry\_out/overflow for your whole 4-bit adder.
4. **Test bench** using Verilog to test your circuit. You do not need all cases in the test bench. Just pick two input numbers and see if the addition is correct. It is good to have one case where there is overflow (carry\_out of the 4-bit adder is 1). Note that, regardless of which design you use (ripple or look-ahead) your test bench codes are same for the 4-bit adder.
5. Implement the **4-bit carry-look-ahead adder in Verilog**. Use the same codes of the previous test bench to check if your design works.
6. Implement the **Verilog 4-bit carry-look-ahead adder in the board**. Use the 8 switches for two 4 bit input numbers and a push button as the carry\_in.

Let me know if you have any question.